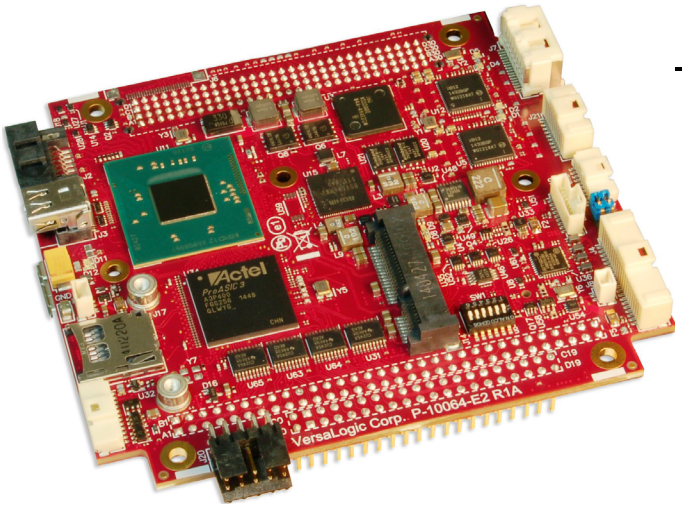
Programmer's Reference Manual

REV. August 2018

BayCat

(VL-EPM-31)



Intel® Atom™-based Single Board Computer with Dual Ethernet, Video, USB, SATA, Serial I/O, Digital I/O, Trusted Platform Module security, Counter/Timers, Mini PCIe, mSATA, PCI/104-*Plus* Interface, and SPX.

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Product Release Notes

Release 1.2

Updated UARTMODE1 – UART MODE REGISTER #1 section.

Release 1.1

Updated Table 39 title.

Release 1

First release of this document.

Support

The EPM-31 support page, at http://www.versalogic.com/private/baycatsupport.asp contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

This is a private page for EPM-31 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

VersaTech KnowledgeBase

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Tables

1 Introduction

This document provides information for users requiring register-level information for developing applications with the VL-EPM-31.

Related Documents

The following documents available are on the EPM-31 Product Support Web Page:

- *EPM-31 Hardware Reference Manual* – provides information on the board's hardware features including connectors and all interfaces.
- *EPM-31 BIOS Reference Manual* – provides information on accessing and configuring settings in the BIOS Setup utility. All BIOS menus, submenus, and configuration options are described.

This document is available through the software page:

- *VersaAPI Installation and Reference Guide* – describes the shared library of API calls for reading and controlling on-board devices on certain VersaLogic products.

System Resources and Maps

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Memory Map

Table 1: Memory Map

Address Range	Description
00000h – 9FFFFh	Legacy system (DOS) area
A0000h – B7FFFh	ISA memory area (VGA frame buffer is not accessible)
B8000h – BFFFFh	Text mode buffer
C0000h – CFFFFh	Video BIOS area
D0000h – DFFFFh	PCI ROM expansion area
E0000h – FFFFFh	Legacy BIOS (reserved)

Interrupts

The LPC SERIRQ is used for interrupt interface to the BayTrail SoC.

Each of the following devices can have an IRQ interrupt assigned to it and each with an interrupt enable control for IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, and IRQ11:

- 8254 timers (with three interrupt status bits)
- 16 digital I/Os (with 16 interrupt status bits)
- 8 AUX GPIOs (with one interrupt status bit)
- COM 1 UART (with 16550 interrupt status bits)
- COM 2 UART (with 16550 interrupt status bits)
- Watchdog timer (one status bit)
- SPX expansion interface (status is determined by the devices on this interface). This uses selects from four of the “usual” IRQs.
- Thermal event and battery-low interrupts
- ISA interrupts

The ISA bus supports 11 interrupts: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, and IRQ15. There is an interrupt enable control for each and by default they are all disabled. ISA bus interrupts simply pass through to the SERIRQ (no capture in the FPGA).

Common interrupts can be assigned to multiple devices if software can deal with it (this is common on UARTs being handled by a common ISR).

Interrupt status bits for everything except the UARTs will “stick” and are cleared by a “write-one” to a status register bit. The 16550 UART interrupts behave as defined for the 16550 registers and are a pass-through to the LPC SERIRQ.

Per the VersaAPI standard, anytime an interrupt on the SERIRQ is enabled, the slot becomes active. All interrupts in the SERIRQ are high-true so when the slot becomes active, the slot will be low when there is no interrupt and high when there is an interrupt.

Table 2: I/O Map

I/O Address Range	Device/Owner
2F8h – 2FFh	COM2 serial port default
3B0h – 3DFh	Legacy VGA registers
3F8h – 3FFh	COM1 serial port default
400h – 47Fh	ACPI / Power management (reserved)
500h – 5FFh	PCH GPIO (reserved)
C80h – CBBh	EPM-31 FPGA Board Control Registers
CBCh – CBFh	EPM-31 FPGA 8254 Timer Registers

FPGA I/O Space

The FPGA is mapped into I/O space on the LPC bus. The only other device on the LPC bus is the Trusted Platform Module (TPM), but it is a memory-mapped device that is not allowed to use I/O space. The address range is mapped into 64 byte I/O window.

- FPGA access: LPC I/O space
- FPGA access size: All 8-bit byte accesses (16-bit like registers are aligned on 16-bit word boundaries to make word access possible in software but the LPC bus still splits the accesses into two 8-bit accesses)
- FPGA address range: 0xC80 to 0xCBF (64-byte window)

The three 8254 timers only require four bytes of addressing and are located at the end of the 64-byte I/O block. The only requirement is that the base address must be aligned on a 4-byte block. Table 3 lists the FPGA's I/O map.

Table 3: FPGA I/O Map

Address Range	Device	Size
0xC80 – 0xCBB	FPGA registers	60 bytes
0xCBC – 0xCBF	8254 timer address registers	4 bytes

ISA Bus Addressing and LPC I/O and Memory Map

The FPGA implements an LPC-to-ISA bridge. The LPC bus only has the FPGA and the TPM device on it. The TPM is a memory mapped device at base address 0xFED40000. The FPGA uses I/O space 0xC80-0xCBF. The ISA bus memory address space is16 Mbytes (24-bits of address); ISA busy I/O addressing is limited to 64 Kbytes (16 bits of address). As such, the following will be the allowed memory and I/O map for the ISA bus.
All LPC I/O cycles that are unclaimed by the FPGA will pass through to the ISA bus. Similarly, all LPC memory cycles below 16 Mbytes will be passed through to the ISA bus.

Table 4: ISA Bus I/O Map

Address Range	Device	Size
0xC80 - 0xCBF	FPGA registers	64 bytes
All other LPC I/O cycles	ISA bus	Depends on SoC LPC I/O traffic

Table 5: ISA Memory Map

Address Range	Device	Size
0x0 – 0xFFFFFF LPC memory cycles	ISA bus	Depends on SoC LPC memory traffic
0x1000000 and higher LPC memory cycles	Ignored by FPGA	TPM is the only memory device on the LPC bus

FPGA Register Map

Register Access Key	
R/W	Read/Write
RO	Read-only (status or reserved)
R/WC	Read-status/Write-1-to-Clear
RSVD	Reserved. Only write 0 to this bit; ignore all read values.

Reset Status Key	
POR	Power-on reset (only resets one time when input power comes on)
Platform	Resets prior to the processor entering the S0 power state (that is, at power-on and in sleep states)
resetSX	• If FPGA_PSEN is a '0' in MISCSR1 (default setting), then this is the same as the Platform reset. • If FPGA_PSEN is a programmed to a '1', then it is the same as the Power-On Reset (POR).
n/a	Reset doesn't apply to status or reserved registers

Identifier	I/O Address	Offset	Reset Type	D7	D6	D5	D4	D3	D2	D1	D0
PCR	C80	0	Platform	PLED	PRODUCT_CODE						
PSR	C81	1	n/a	REV_LEVEL					EXTEMP	CUSTOM	BETA
SCR	C82	2	Platform	BIOS_JMP	BIOS_OR	BIOS_SEL	LED_DEBUG	WORKVER	RSVD	RSVD	RSVD
TICR	C83	3	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	RSVD	IMASK_TC5	IMASK_TC4	IMASK_TC3
TISR	C84	4	Platform	RSVD	RSVD	RSVD	RSVD	RSVD	ISTAT_TC5	ISTAT_TC4	ISTAT_TC3
TCR	C85	5	Platform	TIM5GATE	TIM4GATE	TIM3GATE	TM45MODE	TM4CLKSEL	TM3CLKSEL	RSVD	TMRFULL
Reserved	C86	6	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reserved	C87	7	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
SPICONTROL	C88	8	Platform	CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0
SPISTATUS	C89	9	Platform	IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY
SPIDATA0	C8A	A	Platform	MSB	<==========						LSB
SPIDATA1	C8B	B	Platform	MSB	<==========						LSB
SPIDATAT2	C8C	C	Platform	MSB	<==========						LSB
SPIDATA3	C8D	D	Platform	MSB	<==========						LSB
SPIMISC	C8E	E	Platform	RSVD	MUXSEL2	MUXSEL1	MUXSEL0	RSVD	SERIRQEN	SPILB	RSVD
Reserved	C8F	F	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
MISCSCR1	C90	10	POR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FPGA_PSEN	MINI_PSDIS

Identifier	I/O Address	Offset	Reset Type	D7	D6	D5	D4	D3	D2	D1	D0
MISCSR2	C91	11	POR	USB_HUBMODE	W_DISABLE	ETH1_OFF	ETH0_OFF	USB_USBID	USB_HUBDIS	USB_PBDIS	USB_OBDIS
MISCSR3	C92	12	Platform	RSVD	RSVD	RSVD	RSVD	USB_PBOC	PBRESET	RSVD	RSVD
Reserved	C93	13	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
DIODIR1	C94	14	resetSX	DIR_DIO8	DIR_DIO7	DIR_DIO6	DIR_DIO5	DIR_DIO4	DIR_DIO3	DIR_DIO2	DIR_DIO1
DIODIR2	C95	15	resetSX	DIR_DIO16	DIR_DIO15	DIR_DIO14	DIR_DIO13	DIR_DIO12	DIR_DIO11	DIR_DIO10	DIR_DIO9
DIOPOL1	C96	16	resetSX	POL_DIO8	POL_DIO7	POL_DIO6	POL_DIO5	POL_DIO4	POL_DIO3	POL_DIO2	POL_DIO1
DIOPOL2	C97	17	resetSX	POL_DIO16	POL_DIO15	POL_DIO14	POL_DIO13	POL_DIO12	POL_DIO11	POL_DIO10	POL_DIO9
DIOOUT1	C98	18	resetSX	OUT_DIO8	OUT_DIO7	OUT_DIO6	OUT_DIO5	OUT_DIO4	OUT_DIO3	OUT_DIO2	OUT_DIO1
DIOOUT2	C99	19	resetSX	OUT_DIO16	OUT_DIO15	OUT_DIO14	OUT_DIO13	OUT_DIO12	OUT_DIO11	OUT_DIO10	OUT_DIO9
DIOIN1	C9A	1A	n/a	IN_DIO8	IN_DIO7	IN_DIO6	IN_DIO5	IN_DIO4	IN_DIO3	IN_DIO2	IN_DIO1
DIOIN2	C9B	1B	n/a	IN_DIO16	IN_DIO15	IN_DIO14	IN_DIO13	IN_DIO12	IN_DIO11	IN_DIO10	IN_DIO9
DIOMASK1	C9C	1C	Platform	IMASK_DIO8	IMASK_DIO7	IMASK_DIO6	IMASK_DIO5	IMASK_DIO4	IMASK_DIO3	IMASK_DIO2	IMASK_DIO1
DIOMASK2	C9D	1D	Platform	IMASK_DIO16	IMASK_DIO15	IMASK_DIO14	IMASK_DIO13	IMASK_DIO12	IMASK_DIO11	IMASK_DIO10	IMASK_DIO9
DIOSTAT1	C9E	1E	Platform	ISTAT_DIO8	ISTAT_DIO7	ISTAT_DIO6	ISTAT_DIO5	ISTAT_DIO4	ISTAT_DIO3	ISTAT_DIO2	ISTAT_DIO1
DIOSTAT2	C9F	1F	Platform	ISTAT_DIO16	ISTAT_DIO15	ISTAT_DIO14	ISTAT_DIO13	ISTAT_DIO12	ISTAT_DIO11	ISTAT_DIO10	ISTAT_DIO9
DIOCR	CA0	20	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	RSVD	RSVD	RSVD	TMREN
AUXDIR	CA1	21	resetSX	DIR_GPIO8	DIR_GPIO7	DIR_GPIO6	DIR_GPIO5	DIR_GPIO4	DIR_GPIO3	DIR_GPIO2	DIR_GPIO1
AUXPOL	CA2	22	resetSX	POL_GPIO8	POL_GPIO7	POL_GPIO6	POL_GPIO5	POL_GPIO4	POL_GPIO3	POL_GPIO2	POL_GPIO1
AUXOUT	CA3	23	resetSX	OUT_GPIO8	OUT_GPIO7	OUT_GPIO6	OUT_GPIO5	OUT_GPIO4	OUT_GPIO3	OUT_GPIO2	OUT_GPIO1
AUXIN	CA4	24	n/a	IN_GPIO8	IN_GPIO7	IN_GPIO6	IN_GPIO5	IN_GPIO4	IN_GPIO3	IN_GPIO2	IN_GPIO1
AUXIMASK	CA5	25	Platform	IMASK_GPIO8	IMASK_GPIO7	IMASK_GPIO6	IMASK_GPIO5	IMASK_GPIO4	IMASK_GPIO3	IMASK_GPIO2	IMASK_GPIO1
AUXISTAT	CA6	26	Platform	ISTAT_GPIO8	ISTAT_GPIO7	ISTAT_GPIO6	ISTAT_GPIO5	ISTAT_GPIO4	ISTAT_GPIO3	ISTAT_GPIO2	ISTAT_GPIO1
AUXMODE1	CA7	27	resetSX	MODE_GPIO8	MODE_GPIO7	MODE_GPIO6	MODE_GPIO5	MODE_GPIO4	MODE_GPIO3	MODE_GPIO2	MODE_GPIO1
WDT_CTL	CA8	28	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	RSVD	RESET_EN	WDT_EN	WDT_STAT
WDT_VAL	CA9	29	Platform	MSB	<==========	==========	==========	==========	==========	==========	LSB
XCVRMODE	CAA	2A	Platform	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	COM2_MODE	COM1_MODE
AUXMODE2	CAB	2B	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	RSVD	RSVD	RSVD	RSVD

Identifier	I/O Address	Offset	Reset Type	D7	D6	D5	D4	D3	D2	D1	D0
FANCON	CAC	2C	Platform	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FAN_OFF
Reserved	CAD	2D	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
FANTACHLS	CAE	2E	Platform	MSB	<==========						LSB
FANTACHMS	CAF	2F	Platform	MSB	<==========						LSB
TEMPICR	CB0	30	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	MASK_BATTLOW	IMASK_EVENT	IMASK_THERM	IMASK_ALERT
TEMPISTAT	CB1	31	Platform	BATTLOW	RSVD	RSVD	RSVD	ISTAT_BATTLOW	ISTAT_EVENT	ISTAT_THERM	ISTAT_ALERT
UART1CR	CB2	32	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	UART1_BASE3	UART1_BASE2	UART1_BASE1	UART1_BASE0
UART2CR	CB3	33	Platform	IRQEN	IRQSEL2	IRQSEL1	IRQSEL0	UART2_BASE3	UART2_BASE2	UART2_BASE1	UART2_BASE0
Reserved	CB4	34	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reserved	CB5	35	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
UARTMODE1	CB6	36	Platform	RSVD	RSVD	UART2_485ADC	UART1_485ADC	RSVD	RSVD	UART2_EN	UART1_EN
UARTMODE2	CB7	37	Platform	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FAST_MODE
ISACON1	CB8	38	Platform	ISA_IRQ11	ISA_IRQ10	ISA_IRQ9	ISA_IRQ7	ISA_IRQ6	ISA_IRQ5	ISA_IRQ4	ISA_IRQ3
ISACON2	CB9	39	Platform	RSVD	RSVD	RSVD	RSVD	RSVD	ISA_IRQ15	ISA_IRQ14	ISA_IRQ12
Reserved	CBA	3A	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Reserved	CBB	3B	n/a	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
8254_ADD0	CBC	3C	Platform	MSB	<==========						LSB
8254_ADD1	CBD	3D	Platform	MSB	<==========						LSB
8254_ADD2	CBE	3E	Platform	MSB	<==========						LSB
8254_ADD3	CBF	3F	Platform	MSB	<==========						LSB

FPGA Register Descriptions

Register Access Key	
R/W	Read/Write
RO	Read-only (status or reserved)
R/WC	Read-status/Write-1-to-Clear
RSVD	Reserved. Only write 0 to this bit; ignore all read values.

PRODUCT INFORMATION REGISTERS

This register drives the PLED on the paddleboard. It also provides read access to the product code.

Table 6: PCR – Product Code and LED Register

Bit	Identifier	Access	Default	Description
7	PLED	R/W	0	Drives the programmable LED on the paddleboard. 0 – LED is off (default) 1 – LED is on (can be used by software)
6-0	PRODUCT_CODE	RO	0010001	Product Code for the EPM-31 (0x11)

Table 7: PSR – Product Status Register

Bit	Identifier	Access	Default	Description
7:3	REV_LEVEL[4:0]	RO	N/A	Revision level of the PLD (incremented every FPGA release) 0 – Indicates production release revision level when BETA status bit (bit 0) is set to '0' 1 – Indicates development release revision level when BETA status bit (bit 0) is set to '1'
2	EXTEMP	RO	N/A	Extended or Standard Temp Status (set via external resistor): 0 – Standard Temp 1 – Extended Temp (probably always set)
1	CUSTOM	RO	N/A	Custom or Standard Product Status (set in FPGA): 0 – Standard Product 1 – Custom Product or PLD/FPGA
0	BETA	RO	N/A	Beta or Production Status (set in FPGA): 1 – Beta (or Debug) 0 – Production

BIOS AND JUMPER STATUS REGISTER

Table 8: SCR –Status/Control Register

Bit	Identifier	Access	Default	Description
7	BIOS_JMP	RO	N/A	Status of the external BIOS switch (jumper): 1 – Primary BIOS selected 0 – Secondary BIOS selected
6	BIOS_OR	R/W	0	BIOS Switch (jumper) Override 0 – BIOS Select will follow the BIOS_JMP switch setting. (**Note**) 1 – BIOS Select will follow the BIOS_SEL register setting
5	BIOS_SEL	R/W	0	BIOS Select (see BIOS_OR): 1 – Primary BIOS selected 0 – Backup BIOS selected
4	LED_DEBUG	R/W	0	Debug LED (controls the yellow LED): 0 – LED is off and follows its primary function (MSATA_DAS) 1 – LED is on (indicates FPGA is programmed by default)
3	WORKVER	RO	N/A	Status used to indicate that the FPGA is not officially released and is still in a working state. 0 – FPGA is released 1 – FPGA is in a working state (not released)
2	RESERVED	RO	N/A	Reserved. Writes are ignored; reads always return 0.
1	RESERVED	RO	N/A	Reserved. Writes are ignored; reads always return 0.
0	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.

Note: This corresponds to the setting of position 6 of the SW1 Configuration Switch block. Refer to the *EPM-31 Hardware Reference Manual* for more information regarding the configuration switches.

TIMER REGISTERS

The FPGA implements an 8254-compatible timer/counter that includes three 16-bit timers.

Table 9: TICR – 8254 Timer Interrupt Control Register

Bit	Identifier	Access	Default	Description
7	IRQEN	R/W	0	8254 Timer interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	8254 Timer interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
2	IMSK_TC5	R/W	0	8254 timer #5 interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled
1	IMSK_TC4	R/W	0	8254 timer #4 interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled
0	IMSK_TC3	R/W	0	8254 timer #3 interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled

Table 10: TISR – 8254 Timer Interrupt Status Register

Bit	Identifier	Access	Default	Description
7	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
6	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
5	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
4	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
3	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
2	ISTAT_TC5	RW/C	N/A	Status for the 8254 Timer #5 output (terminal count) interrupt when read. This bit is read-status and a write-1-to-clear. 0 – Timer output (terminal count) has not transitioned from 0 to a 1 level 1 – Timer output (terminal count) has transitioned from a 0 to a 1 level
1	ISTAT_TC4	RW/C	N/A	Status for the 8254 Timer #4 output (terminal count) interrupt when read. This bit is read-status and a write-1-to-clear. 0 – Timer output (terminal count) has not transitioned from 0 to a 1 level 1 – Timer output (terminal count) has transitioned from a 0 to a 1 level
0	ISTAT_TC3	RW/C	N/A	Status for the 8254 Timer #3 output (terminal count) interrupt when read. This bit is read-status and a write-1-to-clear. 0 – Timer output (terminal count) has not transitioned from 0 to a 1 level 1 – Timer output (terminal count) has transitioned from a 0 to a 1 level

Table 11: TCR – 8254 Timer Control Register

Bit	Identifier	Access	Default	Description
7	TMR5GATE	R/W	0	Debug/Test Only: Controls the "gate" signal on 8254 timer #5 when not using an external gate signal: 0 – Gate on signal GCTC5 is disabled 1 – Gate on signal GCTC5 is enabled Always set to 0 when configuring timer modes except when TMRFULL is '0' and then it should be set to '1' and not changed unless using internal clocking.
6	TMR4GATE	R/W	0	Controls the "gate" signal on 8254 timer #4 when not using an external gate signal: 0 – Gate on signal GCTC4 is disabled 1 – Gate on signal GCTC4 is enabled Always set to 0 when configuring timer modes except when TMRFULL is '0' and then it should be set to '1' and not changed unless using internal clocking
5	TMR3GATE	R/W	0	Controls the "gate" signal on 8254 timer #3 when not using an external gate signal: 0 – Gate on signal GCTC3 is disabled 1 – Gate on signal GCTC3 is enabled Always set to 0 when configuring timer modes except when TMRFULL is '0' and then it should be set to '1' and not changed unless using internal clocking
4	TM45MODE	R/W	0	Mode to set timers #4 and #5 in: 0 – Timer #4 and #5 form one 32-bit timer controlled by timer #1 signals 1 – Timer #4 and Timer #5 are separate 16-bit timers with their own control signals. Almost always used in 32-bit mode especially when TMRFULL is a '0' (the 16-bit timer #5 if of limited use)
3	TM4CLKSEL	R/W	0	Timer #4 Clock Select: 0 – Use internal 4.125 MHz clock (derived from PCI clock) 1 – Use external ICTC4 Timer #5 is always on internal clock if configured as a 16-bit clock
2	TM3CLKSEL	R/W	0	Timer #3 Clock Select: 0 – Use internal 4.125 MHz clock (derived from PCI clock) 1 – Use external ICTC3 assigned to Digital I/O
1	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.
0	TMRFULL	R/W	0	DIOs to use for timer signals (TMREN must be a '1' in the DIOCR register to use the timers). 0 – 4-wire timers and DIO16-DIO13 are external timer control signals 1 – 8-wire and DIO16-DIO9 are external timer control signals Because the gates-controls are not connected to digital I/Os when TMRFULL is a '0', the TIMxGATE gate controls in this register are used so they need to be set to '1' and should not be toggled during operation with external timers (since there is no continuous clock to synchronize them to) but can be toggled if using the internal clock. If you need gating in external modes, set TMRFULL to a '1'.

SPI CONTROL REGISTERS

These are placed at the traditional offset 0x8 location. Only external SPX interface devices use this interface. Because the board uses a 9-pin SPX connector, only two devices are supported.

SPICONTROL

Table 12: SPI Interface Control Register

Bit	Identifier	Access	Default	Description
7	CPOL	R/W	0	SPI clock polarity – Sets the SCLK idle state. 0 – SCLK idles low 1 – SCLK idles high
6	CPHA	R/W	0	SPI clock phase – Sets the SCLK edge on which valid data will be read. 0 – Data is read on rising edge 1 – Data is read on falling edge
5-4	SPILEN(1:0)	R/W	00	Determines the SPI frame length. This selection works in manual and auto slave select modes. 00 – 8-bit 01 – 16-bit 10 – 24-bit 11 – 32-bit
3	MAN_SS	R/W	0	Determines whether the slave select lines are asserted through the user software or are automatically asserted by a write to SPIDATA3. 0 - The slave select operates automatically 1 - The slave select line is controlled manually through SPICONTROL bits SS[2:0]
2-0	SS(2:0)	R/W	000	SPI slave device selection: 000 – None 001 – SS0# 010 – SS1# 011 – Undefined (ignored) 100 – Undefined (ignored) 101 – Undefined (ignored) 110 – Undefined (ignored) 111 – Undefined (ignored)

SPISTATUS

The SPX interrupt is not connected on this product. The control bits and status associated are still defined in the register set but the SPX interrupt will always be de-asserted.

Table 13: SPI Interface Status Register

Bits	Identifier	Access	Default	Description
7-6	IRQSEL[1:0]	R/W	00	The SPX interrupt is not connected on this product (always de-asserted). Selects which IRQ will be enabled if HW_IRQ_EN = 1. Interrupts are not used on this board, so this just becomes a read/write non-functional field. 00 – IRQ3 01 – IRQ4 10 – IRQ5 11 – IRQ10 **Note:** These are the first four interrupts in the "usual" LPC SERIRQ group of eight interrupts.
5-4	SPICLK(1:0)	R/W	00	Selects one of four SCLK frequencies. This is based on a 33 MHz LPC clock. 00 – 1.03125 MHz (33 MHz/32) 01 – 2.0625 MHz (33 MHz/16) 10 – 4.125 MHz (33 MHz/8) 11 – 8.25 MHz (33 MHz/4)
3	HW_IRQ_EN	R/W	0	The SPX interrupt is not connected on this product (always de-asserted). This enables the selected IRQ to be activated by a SPI device that is configured to use its interrupt capability. 0 - IRQs are disabled for SPI operations. 1 - The IRQ can be asserted
2	LSBIT_1ST	R/W	0	Controls the SPI shift direction from the SPIDATA(x) registers. 0 - Data is left-shifted (MSB first). 1 - Data is right-shifted (LSB first)
1	HW_INT	RO	0	SPX interrupt is not connected on this product (always de-asserted). Status flag which indicates when the hardware SPX signal SINT# is asserted. 0 - The hardware interrupt SINT# is de-asserted. 1 - An interrupt is present on SINT# If HW_IRQ_EN= 1, the selected IRQ will also be asserted by the hardware interrupt. HW_INT is read-only and is cleared when the external hardware interrupt is no longer present.
0	BUSY	RO	N/A	Status flag which indicates when an SPI transaction is underway. I2C is so slow that there is no reason to ever poll this. 0 - The SPI bus is idle. 1 - SCLK is clocking data in/out of the SPIDATA(x) registers (that is, busy)

SPI DATA REGISTERS

There are four data registers used on the SPI interface. How many are used depends on the device being communicated with. SPIDATA0 is typically the least significant byte and SPIDATA3 is the most significant byte. Any write to the most significant byte SPIDATA3 initiates the SCLK and, depending on the MAN_SS state, will assert a slave select to begin an SPI bus transaction.

Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first and received data will be shifted in the LSbit of the selected frame size determined by SPILEN1 and SPILEN0. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first and the received data will be shifted in the MSbit of SPIDATA3.

SPIDATA0 (Least Significant Byte)

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

SPIDATA1

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

SPIDATA2

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

SPIDATA3 (Most Significant Byte) [Cycle Trigger Register]

D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB

SPI DEBUG CONTROL REGISTER AND MSATA/PCIE SELECT CONTROL REGISTER

This register is only used to set an SPI loopback (debug/test only) but is also used for the mSATA/PCIe Minicard Mux select.

Table 14: SPI – SPI Debug Control Register

Bit	Identifier	Access	Default	Description
7	Reserved	RO	0	Reserved. Writes are ignored; reads always return 0.
6-4	MUXSEL(2:0)	R/W	000	mSATA/PCIe Mux selection for Minicard slot (and 2nd SATA connector): • 000 – Select mSATA using only pin 43 (MSATA_DETECT). This is an Intel-mode that is reliable for PCIe Minicards but not for mSATA modules that inadvertently ground this signal. • 001 – Use only Pin 51 (PRES_DISABLE2#). This is the default method and is defined in the Draft mSATA spec but some Minicards use it as a second wireless disable. • 010 – Use either Pin 43 or Pin 51. This will work just like 001 because Pin 43 is disabled by an FPGA pull-down. • 011 – Force PCIe mode on the Minicard • 100 – Force mSATA mode on the Minicard. • 101 – Undefined (same as 000) • 110 – Undefined (same as 000) • 111 – Undefined (same as 000) **Note:** When the Minicard uses PCIe, the SATA channel automatically switches to the SATA connector.
3	Reserved	RO	0	Reserved. Writes are ignored; reads always return 0.
2	SERIRQEN	R/W	0	When an IRQ is assigned a slot in the SERIRQ, it will drive the slot with the interrupt state, but this bit must be set to a '1' to do that. 0 – Slots assigned to SERIRQ are not driven (available for other devices). 1 – Slots assigned to SERIRQ are driven with their current interrupt state (which is low since interrupts are high-true). This is because the default interrupt settings in this FPGA can conflict with other interrupts if the VersaAPI is not being used (for example, console redirect using IRQ3).
1	SPILB	R/W	0	Debug/Test Only: Used to loop SPI output data back to the input (debug/test mode). 0 – Normal operation 1 – Loop SPI output data back to the SPI input data (data output still active)
0	RESERVED	RO	0	Reserved. Writes are ignored; reads always return 0.

MISCELLANEOUS FPGA REGISTERS

MISCR1 – Miscellaneous Control Register #1

This is a register in the always-on power well of the FPGA. It holds its state during sleep modes and can only be reset by a power cycle. This is a placeholder register for features like pushing the power-button and also for software initiated resets should those be needed. This register is only reset by the main power-on reset since it must maintain its state in Sleep modes (for example, S3).

Table 15: MISCR1 – Misc. Control Register #1

Bits	Identifier	Access	Default	Description
7-2	Reserved	RO	000000	Reserved. Writes are ignored; reads always return 0.
1	FPGA_PSEN	R/W	0	FPGA digital I/O and AUX GPIO bank I/O power enable 0 – The digital I/O and AUX GPIO bank will be powered down in sleep modes (only power in S0) 1 – The digital I/O and AUX GPIO bank will not be powered down in sleep modes and the configuration will remain. The FPGA 3.3 V I/O bank power switch is controlled by the "OR" of the S0 power control signal and FPGA_PSEN. **Note:** Some register resets are conditional on the state of FPGA_PSEN
0	MINI_PSDIS	R/W	0	Minicard 3.3 V power disable 0 – Minicard 3.3 V power stays on always (this is normally how minicards operate if they support any Wake events) 1 – Minicard 3.3 V power will be turned off when not in S0 (in sleep modes). The Minicard 3.3 V power switch is controlled by the "OR" of the S0 power control signal and the inverse of MINI_PSDIS.

MISCR2 – Miscellaneous Control Register #2

This is a register in the always-on power well of the FPGA. It holds its state during sleep modes and can only be reset by a power cycle. It is primarily used for control signals for the always-powered Ethernet controllers and the USB hubs. This register is only reset by the main power-on reset since it must maintain its state in sleep modes (for example, S3).

Table 16: MISCSR2 – Misc. Control Register #2

Bit	Identifier	Access	Default	Description
7	USB_HUBMODE	R/W	0	Determines whether the hub resets only once (to support wake-up from sleep modes on USB ports) or resets every time it enters sleep modes using the platform reset: 0 – USB hub is reset once at power on. Use USB_HUBDIS to manually control the reset if necessary. This supports USB wake-up modes 1 – USB hub is reset by platform reset every time (will be reset when entering all sleep modes). USB ports cannot be used to wake-up
6	W_DISABLE	R/W	0	Used to control the W_DISABLE (Wireless Disable) signal going to the PCIe Mincard: 0 – W_DISABLE signal is not asserted (Enabled) 1 – W_DISABLE signal is asserted (Disabled) **Note:** There are other control sources that can be configured to control this signal and if enabled the control becomes the "OR" of all sources
5	ETHOFF1	R/W	0	Used to disable the Ethernet controller #1 (controls the ETH_OFF# input to the I210-IT): 0 – Ethernet controller is enabled (On) 1 – Ethernet controller is disabled (Off)
4	ETHOFF0	R/W	0	Used to disable the Ethernet controller #0 (controls the ETH_OFF# input to the I210-IT): 0 – Ethernet controller is enabled (On) 1 – Ethernet controller is disabled (Off)
3	USB_USBID	R/W	0	Set to use the "ID" signal on the on-board USB 3.0 signal to control the VBUS power. USB OTG (on-the-go) uses this signal to tell whether an "A" or "B" cable is plugged in a micro-USB 3.0 "AB" connector. When USB_USBID is set to a '1', an "A" cable will turn VBUS power on and a "B" will turn it off (because "B" devices are not supported). 0 – Do not use "ID" signal to control VBUS power (VBUS power controlled only by USB_OBDIS) 1 – Use "ID" signal to control VBUS power (USB_OBDIS will still disable VBUS power)
2	USB_HUBDIS	R/W	0	Control the reset on the USB2513B Hub. 0 – USB2513 hub is enabled (reset released) 1 – USB2513 hub is in reset
1	USB_PBDIS	R/W	0	Disable control for the paddleboard USB port VBUS power switches (there are two power-switches but they have a common power enable and overcurrent status) 0 – VBUS power switches are enabled 1 – VBUS power switched are disabled. **Note:** The I2164 power switches latch-off in overcurrent and can only be re-enabled by a power-cycle or by setting this bit to a 1, wait >1 ms, and then a 0
0	USB_OBDIS	R/W	0	Disable control for the on-board USB port VBUS power switches (there are two with a common overcurrent): 0 – VBUS power switches are enabled 1 – VBUS power switched are disabled. **Note:** The I2164 power switches latch-off in overcurrent and can only be re-enabled by a power-cycle of by setting this bit to a 1 and then a 0 with at least 1 ms in between

MISCR3 – Miscellaneous Control Register #3

This register sets the SMBus addresses on the 4-Port PCIe Switch.

Table 17: MISCR3 – Misc. Control Register #3

Bits	Identifier	Access	Default	Description
7-4	Reserved	RO	0000	Reserved. Writes are ignored; reads always return 0.
3	USB_PBOC	RO	N/A	Reads the overcurrent status for the USB paddleboard power switches (there are two power switches for the four ports but they have a common overcurrent status). 0 – Overcurrent is not asserted (power switch is on) 1 – Overcurrent is asserted (power switch is off)
2	PBRESET	R/W	---	When written to, this will do the same thing as pushing the reset button, which could be useful for a software-initiated watchdog. 0 – No action 1 – Activate the reset push-button **Note:** Because this generates a reset that will reset this register, it isn't likely a value of a '1' can ever be read-back, so it is somewhat "write-only".
1-0	Reserved	RO	00	Reserved. Writes are ignored; reads always return 0.

DIODIRx (x=1,2) – Digital I/O Direction Control Registers

These two registers control the directions of the 16 digital I/O signals.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a '0' then the reset is the power-on and Platform Reset. If FPGA_PSEN is a '1' then this register is only reset at power-on.

Table 18: DIODIR1 – Digital I/O 8-1 Direction Control Register

Bits	Identifier	Access	Default	Description
7-0	DIR_DIO[8:1]	R/W	0x00	Sets the DIOx direction. For each bit: 0 – Input 1 – Output

Table 19: DIODIR2 – Digital I/O 16-9 Direction Control Register

Bits	Identifier	Access	Default	Description
7-0	DIR_DIO[16:9]	R/W	0x00	Sets the DIOx direction. For each bit: 0 – Input 1 – Output

DIOPOLx (x=1,2) – Digital I/O Polarity Control Registers

These two registers control the polarity of the 16 Digital I/O signals.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a '0' then the reset is the power-on and Platform Reset. If FPGA_PSEN is a '1' then this register is only reset at power-on.

Table 20: DIOPOL1 – Digital I/O 8-1 Polarity Control Register

Bits	Identifier	Access	Default	Description
7-0	POL_DIO[8:1]	R/W	0x00	Sets the DIOx polarity. For each bit: 0 – No polarity inversion 1 – Invert polarity

Table 21: DIOPOL2 – Digital I/O 16-9 Polarity Control Register

Bits	Identifier	Access	Default	Description
7-0	POL_DIO[16:9]	R/W	0x00	Sets the DIOx polarity. For each bit: 0 – No polarity inversion 1 – Invert polarity

DIOOUTx (x=1,2) – Digital I/O Output Control Registers

These two registers set the DIO output value. This value will only set the actual output if the DIO direction is set as an output. Reading this register does not return the actual input value of the DIO (use the DIOIN register for that). As such, this register can actually be used to detect input/output conflicts.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a '0' then the reset is the power-on and Platform Reset. If FPGA_PSEN is a '1' then this register is only reset at power-on.

Table 22: DIOOUT1 – Digital I/O 8-1 Output Control Register

Bits	Identifier	Access	Default	Description
7-0	OUT_DIO[8:1]	R/W	0x00	Sets the DIOx output. For each bit: 0 – De-asserts the output (0 if polarity not inverted, 1 if inverted) 1 – Asserts the output (1 if polarity not-inverted, 0 if inverted)

Table 23: DIOOUT2 – Digital I/O 16-9 Output Control Register

Bits	Identifier	Access	Default	Description
7-0	OUT_DIO[16:9]	R/W	0x00	Sets the DIOx output. For each bit: 0 – De-asserts the output (0 if polarity not inverted, 1 if inverted) 1 – Asserts the output (1 if polarity not-inverted, 0 if inverted)

DIOINx (x=1,2) – Digital I/O Input Status Registers

These two registers set the DIO input value. It will read the input value regardless of the setting on the direction (that is, it always reads the input). This reads the actual state of the DIO pin into the part.

Table 24: DIOIN1 – Digital I/O 8-1 Input Status Register

Bits	Identifier	Access	Default	Description
7-0	IN_DIO[8:1]	RO	N/A	Reads the DIO input status. For each bit: 0 – Input de-asserted if polarity not-inverted; asserted if polarity inverted 1 Input asserted if polarity not-inverted; de-asserted if polarity inverted

Table 25: DIOIN2 – Digital I/O 16-9 Input Status Register

Bits	Identifier	Access	Default	Description
7-0	IN_DIO[16:9]	RO	N/A	Reads the DIO input status. For each bit: 0 – Input de-asserted if polarity not-inverted; asserted if polarity inverted 1 Input asserted if polarity not-inverted; de-asserted if polarity inverted

DIOIMASKx (x=1,2) – Digital I/O Interrupt Mask Registers

These two registers are the interrupt mask registers for the digital IOs. The reset type is Platform Reset because interrupts always have to be setup after exiting sleep states.

Table 26: DIOIMASK1 – Digital I/O 8-1 Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	IMASK_DIO[8:1]	R/W	0	Digital I/O 8-1 interrupt mask. For each bit: 0 – Interrupt disabled 1 – Interrupt enabled

Table 27: DIOIMASK2 – Digital I/O 16-9 Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	IMASK_DIO[16:9]	R/W	0	Digital I/O 16-9 interrupt mask. For each bit: 0 – Interrupt disabled 1 – Interrupt enabled

DIOISTATx (x=1,2) – Digital I/O Interrupt Status Registers

Table 28: DIOISTAT1 – Digital I/O 8-1 Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	ISTAT_DIO[8:1]	RW/C	N/A	DIOx interrupt status. A read returns the interrupt status. Writing a '1' clears the interrupt status. This bit is set to a '1' on a transition from low-to-high (POL_DIOx=0) or high-to-low (POL_DIOx=1).

Table 29: DIOISTAT2 – Digital I/O 16-9 Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	ISTAT_DIO[16:9]	RW/C	N/A	DIOx interrupt status. A read returns the interrupt status. Writing a '1' clears the interrupt status. This bit is set to a '1' on a transition from low-to-high (POL_DIOx=0) or high-to-low (POL_DIOx=1).

DIOCR – Digital I/O Control Register

One interrupt can be generated for the 16 digital I/Os. Reset type is Platform.

Table 30: DIOCR – Digital I/O Control Register

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	DIO interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	DIO interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-1	RESERVED	RO	000	Reserved. Writes are ignored; reads always return 0.
0	TMREN	R/W	0	Timer enable signals (used to switch digital I/Os to timer control signals): 0 – Timers disabled 1 – Timers enabled and some DIOs are used based on the TMRFULL setting in the Timer control register (TCR)

AUXDIR – AUX GPIO Direction Control Register

This register controls the direction of the eight AUX GPIO signals.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a '0' then the reset is the power-on and Platform Reset. If FPGA_PSEN is a '1' then this register is only reset at power-on.

Table 31: AUXDIR – AUX GPIO Direction Control Register

Bit	Identifier	Access	Default	Description
7-0	DIR_GPIO[8:1]	R/W	0	Sets the direction of the AUX GPIOx lines. For each bit: 0 – Input 1 – Output

AUXPOL – AUX GPIO Polarity Control Register

This register controls the polarity of the eight AUX GPIO signals.

This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a '0' then the reset is the power-on and Platform Reset. If FPGA_PSEN is a '1' then this register is only reset at power-on.

Table 32: AUXPOL – AUX GPIO Polarity Control Register

Bits	Identifier	Access	Default	Description
7-0	POL_GPIO[8:1]	R/W	0	Sets the polarity of the AUX GPIOx lines. For each bit: 0 – No inversion 1 – Invert **Note:** This impacts the polarity as well as the interrupt status edge used.

AUXOUT – AUX GPIO Output Control Register

This register sets the AUX GPIO output value. This value will only set the actual output if the GPIO direction is set as an output. Reading this register does not return the actual input value of the GPIO (use the AUXIN register for that). As such, this register can actually be used to detect input/output conflicts.
This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a '0' then the reset is the power-on and Platform Reset. If FPGA_PSEN is a '1' then this register is only reset at power-on.

Table 33: AUXOUT – AUX GPIO Output Control Register

Bits	Identifier	Access	Default	Description
7-0	OUT_GPIO[8:1]	R/W	0	Sets the AUX GPIOx output values. For each bit: 0 – De-asserts the output (0 if polarity not-inverted, 1 if inverted) 1 – Asserts the output (1 if polarity not-inverted, 0 if inverted)

AUXIN – AUX GPIO I/O Input Status Register

This registers sets the AUX GPIO input value. It will read the input value regardless of the setting on the direction (that is, it always reads the input). This reads the actual state of the GPIO pin into the part.

Table 34: AUXIN – AUX GPIO Input Status Register

Bits	Identifier	Access	Default	Description
7-0	IN_GPIOIO[8:1]	RO	N/A	Reads the GPIOx input status. For each bit: 0 – Input de-asserted if polarity not-inverted; asserted if polarity inverted 1 Input asserted if polarity not-inverted; de-asserted if polarity inverted

AUXIMASK – AUX GPIO Interrupt Mask Register

This is the interrupt mask registers for the AUX GPIOs and the interrupt enable selection. The reset type is Platform Reset because interrupts always have to be setup after exiting sleep states.

Table 35: AUXICR – AUX GPIO Interrupt Mask Register

Bits	Identifier	Access	Default	Description
7-0	IMASK_GPIO[8:1]	R/W	0	GPIOx interrupt mask. For each bit: 0 – Interrupt disabled 1 – Interrupt enabled

AUXISTAT – AUX GPIO I/O Interrupt Status Register

Table 36: AUXISTAT – AUX GPIO Interrupt Status Register

Bits	Identifier	Access	Default	Description
7-0	ISTAT_GPIO[8:1]	RW/C	N/A	GPIOx interrupt status. A read returns the interrupt status. Writing a '1' clears the interrupt status. This bit is set to a '1' on a transition from low-to-high (POL_DIOx=0) or high-to-low (POL_DIOx=1).

AUXMODE1– AUX I/O Mode Register #1

These two registers selected the mode on each AUX GPIO. This reset depends on the state of the FPGA_PSEN signal. If FPGA_PSEN is a '0' then the reset is the power-on and Platform Reset. If FPGA_PSEN is a '1' then this register is only reset at power-on.

Table 37: AUXMODE1 – AUX I/O Mode Register

Bit	Identifier	Access	Default	Description
7	MODE_GPIO8	R/W	0	GPIO8 mode. 0 – GPIO (I/O) 1 – W_DISABLE (input). In this mode, the GPIO is passed through to the W_DISABLE# signal. The GPIO polarity control applies. The GPIO input status can still be read.
6	MODE_GPIO7	R/W	0	GPIO7 mode. 0 – GPIO (I/O) 1 – SLEEP (output). In this mode, the GPIO indicates that the CPU is in a sleep mode (S3 or higher). The GPIO polarity control applies. The GPIO input status can still be read.
5	MODE_GPIO6	R/W	0	GPIO6 mode. 0 – GPIO (I/O) 1 – PWM0 from BayTrail SoC (output). In this mode, the GPIO tracks the PWM0 signal from the BayTrail SoC. The GPIO polarity control applies. The GPIO input status can still be read.
4	MODE_GPIO5	R/W	0	GPIO5 mode. 0 – GPIO (I/O) 1 – Power Good (output). In this mode, the GPIO indicates that the board is in the S0 state and all power is good. The GPIO polarity control applies. The GPIO input status can still be read.
3	MODE_GPIO4	R/W	0	GPIO4 mode. 0 – GPIO (I/O) 1 – Watchdog Reset (output). In this mode, the GPIO will be the watchdog timer trigger output that signals external equipment that the watchdog fired. The GPIO polarity control applies. The GPIO input status can still be read.
2	MODE_GPIO3	R/W	0	GPIO3 mode. 0 – GPIO (I/O) 1 – Reserved for future secondary mode (do not set)
1	MODE_GPIO2	R/W	0	GPIO2 mode. 0 – GPIO (I/O) 1 – Reserved for future secondary mode (do not set)
0	MODE_GPIO1	R/W	0	GPIO1 mode. 0 – GPIO (I/O) 1 – Reserved (same as GPIO)

WDT_CTL – Watchdog Control Register

Reset type is Platform.

Table 38: WDT_CTL – Watchdog Control Register

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	Watchdog interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	Watchdog interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3	Reserved	RO	0	Reserved. Writes are ignored; reads always return 0.
2	RESET_EN	R/W	0	Enable the Watchdog to assert the push-button reset if it “fires”. 0 – Watchdog will not reset the board 1 – Board will be reset if the Watchdog “fires”
1	WDT_EN	R/W	0	Watchdog Enable: 0 – Watchdog is disabled 1 – Watchdog is enabled **Note:** The WDT_VAL register must be set before enabling.
0	WDT_STAT	RO	0	Watchdog Status: 0 – Watchdog disabled or watchdog has not “fired” 1 – Watchdog fired. **Note:** Once set to a ‘1’, it will remain so until any of the following occurs: • the WDT_VAL register is written to • the WDT_EN is disabled • a reset occurs

WDT_VAL – Watchdog Value Register

This register sets the number of seconds for a Watchdog prior to enabling the watchdog. By writing this value, the watchdog can be prevented from "firing". A watchdog fires whenever this registers value is all 0s, so it must be set to a non-zero value before enabling the watchdog to prevent an immediate "firing". Reset type is Platform.

The value written should always be 1 greater than the desired timeout value due to a 0-1 second "tick" error band (values written should range from 2-255 because a 1 could cause an immediate trigger); that is, the actual timeout is WDT_VAL seconds with a -1 second to 0 second error band.

Table 39: WDT_VAL – Watchdog Value Register

Bits	Identifier	Access	Default	Description
7-0	WDT_VAL(7:0)	R/W	0x00	Number of seconds before the Watchdog fires. By default, it is set to zero which results in an immediate watchdog if WDT_EN is set to a '1'.

XCVRMODE – COM Transceiver Mode Register

Sets the RS232 vs RS422/485 mode on the COM port Transceivers. These drive the UART_SEL signals from the FPGA to the Transceivers.
Reset type is Platform.

Note: The values shown are for the default BIOS configuration.

Table 40: XCVRMODE – COM Transceiver Mode Register

Bits	Identifier	Access	Default	Description
7-4	Reserved	RO	0000	Reserved. Writes are ignored; reads always return 0.
3-2	Reserved	RO	00	Reserved. Writes are ignored; reads always return 0.
1	COM2_MODE	R/W	0	COM2 Transceiver mode: 0 – RS232 1 – RS422/485
0	COM1_MODE	R/W	0	COM1 Transceiver mode: 0 – RS232 1 – RS422/485

AUXMODE2– AUX I/O Mode Register #2

This register defines the interrupt mapping for the AUX GPIOs. Reset type is Platform.

Table 41: AUXMODE2 - AUX I/O Mode Register #2

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	AUX GPIO interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	AUX GPIO interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-0	Reserved	RO	0000	Reserved. Writes are ignored; reads always return 0.

FANCON – Fan Control Register

The fan is always off in any sleep mode. When the processor comes out of a sleep state, this register must be setup again since it will be reset to default by the platform reset signal. The fan is always turned “off” in sleep modes. No PWM fan control is supported on the EPM-31. Reset type is Platform.

Note: The BIOS (via ACPI) may modify this register when in an ACPI-capable operating system. The register can be read for status purposes but do not write to it unless you are using a non-ACPI operating system.

Table 42: FANCON – Fan Control Register

Bits	Identifier	Access	Default	Description
7-1	Reserved	RO	0000000	Reserved. Writes are ignored; reads always return 0.
0	FAN_OFF	R/W	0	Fan enable: 0 – Fan is on 1 – Fan is off

FANTACHLS, FANTACHMS – Fan Tach Status Registers

These registers contain the number of fan tach output samples over a one-second sampling period. The value is always valid after the fan speed stabilizes and is updated every 1 second (after a delay of 1 second). Currently, only the lower 10-bits have a valid tach reading (that is, the upper 6 bits will always be zero). The fan tach count should never overflow in the one second period, but it if does, the value will "stick" at 0x03FF.

The board can handle up at least a 10,000 RPM fan with a fan tach output of up to four uniform pulses per revolution. The duty cycle of the fan tach output pulse can be as low as 25% (typically they are very close to 50%). The conversion to RPM is as follows:

RPM = (FANTACH x 60) / PPR

Where…

- FANTACH - the 16-bit register reading
- PPR – fan tach pulses per revolution (typically either 1, 2, or 4)

Reset type is n/a.

Table 43: FANTACHLS – FANTACH Status Register Least Significant Bits

Bits	Identifier	Access	Default	Description
7-0	FANTACH[7:0]	RO	N/A	Least significant eight bits of FANTACH. Read this register first since it latches the value for the most significant eight bits.

Table 44: FANTACHMS – FANTACH Status Register Most Significant Bits

Bits	Identifier	Access	Default	Description
7-0	FANTACH[15:8]	RO	N/A	Most significant eight bits of FANTACH. Read this register after reading FANTACHLS.

Integrator's Note:

The FANTACHLS register must be read first. It will latch a copy of the MS bits so that when FANTACHMS is read, it is based on the same 16-bit value. This assumes that a 16-bit word read on the LPC bus reads the even (LS) address before the odd (MS) address.

TEMPICR – Temperature Interrupt Control Register

This is the interrupt mask register for the temperature sensor thermal alerts and the DDR3 SODIMM EVENT signals and the interrupt enable and selection. The SODIMM may not have any temperature event capability. Reset type is Platform.

Table 45: TEMPICR – Temperature Interrupt Control Register

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	Temperature interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	Temperature interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3	IMASK_BATTLOW	R/W	0	Battery-low interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled.
2	IMASK_EVENT	R/W	0	SODIMM EVENT output interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled.
1	IMASK_THERM	R/W	0	Temperature Sensor THERM output interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled.
0	IMASK_ALERT	R/W	0	Temperature Sensor ALERT output interrupt mask: 0 – Interrupt disabled 1 – Interrupt enabled.

TEMPISTAT – Temperature Interrupt Status Register

Reset type: n/a.

Table 46: TEMPISTAT – Temperature Interrupt Status Register

Bits	Identifier	Access	Default	Description
7	IN_BATTLOW	RO	N/A	Reads the battery low input status. 0 – battery-low is de-asserted (battery is OK) 1 – battery-low is asserted (battery is low)
6-4	Reserved	RO	000	Reserved. Writes are ignored; reads always return 0.
3	ISTAT_BATTLOW	RW/C	N/A	Battery-Low interrupt status. A read returns the interrupt status. Writing a '1' clears the interrupt status. This bit is set to a '1' on a transition from de-asserted-to-asserted
2	ISTAT_EVENT	RW/C	N/A	SODIMM EVENT interrupt status. A read returns the interrupt status. Writing a '1' will clear the interrupt status
1	ISTAT_THERM	RW/C	N/A	Temperature Sensor THERM interrupt status. A read returns the interrupt status. Writing a '1' clears the interrupt status
0	ISTAT_ALERT	RW/C	N/A	Temperature Sensor ALERT interrupt status. A read returns the interrupt status. Writing a '1' clears the interrupt status

UART1CR – UART1 Control Register (COM1)

Reset type is Platform.

Note: The BIOS (via ACPI) may modify this register when in an ACPI-capable operating system. The register can be read for status purposes but do not write to it unless you are using a non-ACPI operating system.

Table 47: UART1CR – UART1 Control Register (COM1)

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	UART interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	001	UART interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 001 – IRQ4 **[← COM1 Default]** 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-0	UART1_BASE(3:0)	R/W	0000	UART Base Address: 0000 - 3F8h **[← COM1 Default]** 0001 - 2F8h 0010 - 3E8h 0011 - 2E8h 0100 - 200h 0101 - 208h 0110 - 220h 0111 - 228h 1000 - 238h 1001 - 338h 1010-1111 **[← These values are reserved; do not use.]**

UART2CR – UART2 Control Register (COM2)

Reset type is Platform.

Note: The BIOS (via ACPI) may modify this register when in an ACPI-capable operating system. The register can be read for status purposes but do not write to it unless you are using a non-ACPI operating system.

Table 48: UART2CR – UART2 Control Register (COM2)

Bits	Identifier	Access	Default	Description
7	IRQEN	R/W	0	UART interrupt enable/disable: 0 – Interrupts disabled 1 – Interrupts enabled
6-4	IRQSEL(2:0)	R/W	000	UART interrupt IRQ select in LPC SERIRQ: 000 – IRQ3 **[← COM2 Default]** 001 – IRQ4 010 – IRQ5 011 – IRQ10 100 – IRQ6 101 – IRQ7 110 – IRQ9 111 – IRQ11
3-0	UART2_BASE(3:0)	R/W	0001	UART Base Address: 0000 - 3F8h 0001 - 2F8h **[← COM2 Default]** 0010 - 3E8h 0011 - 2E8h 0100 - 200h 0101 - 208h 0110 - 220h 0111 - 228h 1000 - 238h 1001 - 338h 1010-1111 **[← These values are reserved; do not use.]**

UARTMODE1 – UART MODE REGISTER #1

When the COM Transceiver Mode is set to RS422/485 (in the XCVRMODE register) and the RS-485 Automatic Direction Control is enabled (e.g., UART1_485ADC set to '1') then the transceiver Tx output is enabled when there are bytes to transmit and the transceiver Tx output is disabled (i.e., tri-stated) when there are no bytes to transmit.

When the COM Transceiver Mode is set to RS422/485 and Automatic Direction Control is disabled (e.g., UART1_485ADC set to '0') then the UART is in Manual Direction Control mode and the transceiver Tx output enable is controlled by software using the RTS bit in the UART Modem Control Register.
RTS = '0' - Transceiver Tx output is enabled.
RTS = '1' - Transceiver Tx output is disabled (i.e., tri-stated).

Reset type is Platform.

Note: Terminal software, expecting an RS-232 port, may set RTS to '1' and disable the transmitter when initializing an RS-422/485 port in Manual Direction Control mode. Application software that handles the RS-422/485 port should set RTS to '0' to enable transmitting when in Manual Direction Control mode.

Table 49: UARTMODE1 – UART MODE Register #1

Bits	Identifier	Access	Default	Description
7-6	Reserved	RO	00	Reserved. Writes are ignored; reads always return 0.
5	UART2_485ADC	R/W	0	COM2 RS-485 Automatic Direction Control: 0 – Disabled 1 – Enabled **Note:** Only enable in RS-485 mode. The COM2_MODE in XCVRMODE register must also be set to a '1'
4	UART1_485ADC	R/W	0	COM1 RS-485 Automatic Direction Control: 0 – Disabled 1 – Enabled **Note:** Only enable in RS-485 mode. . The COM1_MODE in XCVRMODE register must also be set to a '1'
3-2	Reserved	RO	00	Reserved. Writes are ignored; reads always return 0.
1	UART2_EN	R/W	1	UART #2 Output Enable: 0 – Tx and RTS outputs are disabled and UART I/O accesses are passed to the ISA bus. 1 – Tx and RTS outputs are enabled
0	UART1_EN	R/W	1	UART #1 Output Enable: 0 – Tx and RTS outputs are disabled and UART I/O accesses are passed to the ISA bus 1 – Tx and RTS outputs are enabled

Note:

When a UART is disabled, there will be no decoding of the UART I/O address range and any I/O activity will be passed to the ISA bus (this allows COM ports to be on the

ISA bus if the FPGA UARTs are not used). This means that the UART must be enabled before accessing registers. If this is an issue, separate control bits can be added in UARTMODE2 or make one of the unused UART Base addresses a no-decode.

UARTMODE2 – UART MODE REGISTER #2

Standard software (the BIOS and the operating system) assumes the baud-rate clock is 1.8432 MHz and programs the divisors accordingly; however, a faster oscillator is needed for baud rates higher than 115,200.
The FAST_MODE bit in this register is used to shift the divisor by 4 bits (multiply by 16) so that the legacy baud rate comes out correctly for the 16x UART clock. This bit must be set to use rates above 115,200 and may require custom software.
Reset type is Platform.

Note: The values shown are for the default BIOS configuration.

Table 50: UARTMODE2 – UART MODE Register #2

Bits	Identifier	Access	Default	Description
7-1	Reserved	RO	0000000	Reserved. Writes are ignored; reads always return 0.
0	FAST_MODE	R/W	0	Sets how the baud-rate divisor for the 16550 UARTs are interpreted (applies to all ports): 0 – Divisor is multiplied by 16 (legacy mode for 1.8432 MHz clock) 1 – Divisor is not modified (fast mode for 16x 1.8432 MHz clock) **Note:** This must be set to '1' to use baud rates above 115,200.

ISACONx (x = 1,2) – ISA Control Registers

These register are used to enable ISA interrupts on the LPC SERIRQ. ISA interrupts simply pass through to SERIRQ and - per the ISA bus standard - are always high-true. The SERIRQEN control bit is not used for the ISA interrupt mask and should not be set until the interrupt processing is ready.

Note: The values shown are for the default BIOS configuration.

Table 51: ISACON1 – ISA Control Register #1

Bits	Identifier	Access	Default	Description
7	ISA_IRQ11	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
6	ISA_IRQ10	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
5	ISA_IRQ9	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
4	ISA_IRQ7	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
3	ISA_IRQ6	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
2	ISA_IRQ5	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
1	ISA_IRQ4	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
0	ISA_IRQ3	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ

Table 52: ISACON2 – ISA Control Register #2

Bits	Identifier	Access	Default	Description
7	RSVD	RSVD	0	Reserved. Only write 0 to this bit; ignore all read values.
6-3	Reserved	RO	0	Reserved. Writes are ignored; reads always return 0.
2	ISA_IRQ15	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
1	ISA_IRQ14	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ
0	ISA_IRQ12	R/W	0	Interrupt enable for ISA interrupt 0 – Do not pass ISA interrupt to SERIRQ 1 – Pass ISA interrupt to SERIRQ

4 Programming Information for Hardware Interfaces

Processor WAKE# Capabilities

The following devices can wake up the processor using the PCIE_WAKE# signal to the SoC:

- Ethernet port 0 controller
- Ethernet port 1 controller
- Minicard (when always-powered)
- FPGA via the AUX connector GPIO(3) secondary function

The following USB devices can wake up the processor using the in-band SUSPEND protocol:

- On-board USB 3.0 port
- Any of the three Paddleboard USB Ports via the USB2513B Hub
- The USB 2.0 port on the paddleboard that directly connects to the Baytrail SoC
- Minicard (when +3.3 V power is left on during sleep modes)

Watchdog Timer

A Watchdog timer is implemented within the FPGA. When triggered, the Watchdog timer can set a status bit, generate an interrupt and/or hit the push-button-reset. The Watchdog timer implements a 1-255 second timeout.

The Watchdog time out is set in an 8-bit register (WDT_VAL). When the Watchdog is enabled, the WDT_VAL will start to count down. If the Watchdog is enabled and whenever WDT_VAL is zero, the Watchdog is triggered (so a non-zero value must be written before enabling the watchdog). Software must periodically write a non-zero value to WDT_VAL to prevent this trigger. The value written should always be 1 greater than the desired timeout value due to a 0-1 second error band. Values written should be from 2-255 because a 1 could cause an immediate trigger); that is, the actual timeout is WDT_VAL seconds with a -1 second to 0 second error band.

The Watchdog control/status register(s) have bits for the following:

- Watchdog enable/disable (disabled by default)
- Watchdog timeout status (This is cleared when the Watchdog is disabled or when a new value is written to WDT_VAL. Writing WDT_VAL would be the interrupt-acknowledge.)
- Watchdog interrupt IRQ select (from the same list of eight interrupts supported on the LPC SERIRQ)
- Interrupt enable
- Board reset enable (when set, the board will be reset when the Watchdog timer expires).

Industrial I/O Functions and SPI Interface

The EPM-31 employs a set of I/O registers for controlling external serial peripheral interface (SPI) devices. Refer to the descriptions of the SPICONTROL (page 13), SPISTATUS (page 14), and SPIDATA[0:3] (page 15) registers for more information.

The SPI bus specifies four logic signals:

- SCLK – Serial clock (output from master)
- MOSI – Master output, slave input (output from master)
- MISO – Master input, slave output (output from slave)
- SS – Slave select (output from master)

The EPM-31 SPI implementation adds additional features, such as hardware interrupt input to the master. The master initiates all SPI transactions. A slave device responds when its slave select is asserted and it receives clock pulses from the master.

Slave selects are controlled in one of two modes: manual or automatic. In automatic mode, the slave select is asserted by the SPI controller when the most significant data byte is written. This initiates a transaction to the specified slave device. In manual mode, the slave select is controlled by the user and any number of data frames can be sent. The user must command the slave select high to complete the transaction.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. All four common SPI modes are supported through the use of clock polarity and clock phase controls.

To initiate an SPI transaction, configure SPI registers SPICONTROL and SPISTATUS as shown in Table 12 and Table 13 for the desired I/O device. For additional information on communicating with specific SPI devices, refer to their respective manufacturer's datasheets.

Programmable LED

User I/O connector J4 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J4, pin 16; connect the anode to +3.3 V. An on-board resistor limits the current when the circuit is turned on. A programmable LED is provided on the CBR-4005B paddleboard. Refer to the *EPM-31 Hardware Reference Manual* for the location of the Programmable LED on the CBR-4005B paddleboard.

To switch the PLED on and off, refer to Table 6: PCR – Product Code and LED Register, on page 8.

**** End of document ****